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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/891,925	06/27/2001	Mitsuhiro Yano	198786US2 RE	3745

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EXAMINER	
HU, SHOUXIANG	
ART UNIT	**PAPER NUMBER**
2811	

NOTIFICATION DATE	DELIVERY MODE
03/24/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	09/891,925	YANO ET AL.	
	Examiner	Art Unit	
	Shouxiang Hu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Reissue Applications

Applicant is reminded of the continuing obligation under 37 CFR 1.178(b), to timely apprise the Office of any prior or concurrent proceeding in which Patent No. 5,945,692 is or was involved. These proceedings would include interferences, reissues, reexaminations, and litigation.

Applicant is further reminded of the continuing obligation under 37 CFR 1.56, to timely apprise the Office of any information which is material to patentability of the claims under consideration in this reissue application.

These obligations rest with each individual associated with the filing and prosecution of this application for reissue. See also MPEP §§ 1404, 1442.01 and 1442.04.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1 and 12 each recite the subject matters of: a gate forming region; and at least every first gate being formed in the first gate region, but fails to clarify: what is the

relationship between the recited “a gate forming region" and "a first gate region"; and, whether there definitely has only one first gate or definitely have more-than-one first gates formed in the recited first gate region.

Claims 1 and 12 each recite the subject matters that a first semiconductor region of a second conductivity type formed selectively in said first major surface of said first semiconductor layer so that said first conductivity type first semiconductor layer remains along a peripheral portion of said first major surface, and said first conductivity type first semiconductor layer remains in a form of an insular region in a plane view in a central portion of said first major surface. However, they each fail to clarify: Is it the doping state of the first conductivity regions in the first semiconductor layer or the semiconductor layer itself that definitely remains in the recited form of an insular region and/or in the recited central portion? In addition, the recited term of "said first conductivity type first semiconductor layer remains along a peripheral portion of said first major surface” may imply that the entire layer of the first conductivity type first semiconductor layer only remains along the recited peripheral portion; but it should be only a portion of the first conductivity regions of the first semiconductor layer remains in the recited insular form and/or central portion.

Claims 3, 8, 14 and 19 each recite the term of “electrically connected”, but fail to clarify whether it means that the first and second gates are electrically connected to each other or that they are electrically connected to something else.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 7-9, 12-15 and 18-20, insofar as being in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 102(b) as being anticipated by Applicant's admitted prior art ("AAPA").

AAPA discloses a semiconductor device (Figs. 19-21), comprising: a first semiconductor layer (3; N) of a first conductivity type having first and second major surfaces; a first semiconductor region (5 , 11; P) of a second conductivity type formed selectively in said first major surface of said first semiconductor layer; the original/initial doping state of said first semiconductor layer of the first conductivity type remains along/in a peripheral portion of said first major surface and also remains in the form of an insular region (such as the portion or portions of region or regions in layer 3 that is/are between regions 5 under the opening 13) in at least one central portion (the one that is directly under the opening 13) of said first major surface in a plane view; a second semiconductor region (6, under the opening 13; N) of the first conductivity type formed in a surface of said first semiconductor region, with a channel region provided between said second semiconductor region and said insular region of said first semiconductor layer; a gate insulating film (7) formed on a surface of said channel region; a gate forming region including a first gate forming region (the gate forming

region that is under and/or near the opening 13) having one or more than one first gates formed on said gate insulating film and formed substantially adjacent (i.e., substantially close or near) said peripheral portion; an interlayer insulating film (12) formed at least on said first gate(s); a first main electrode (10) formed over a surface of said interlayer insulating film and covering a surface of said second semiconductor region, said first main electrode being electrically connected to said second semiconductor region and (at least a portion of layer 10) having an end extending to a boundary (any region(s) therebetween or therein) between the peripheral portion of said first major surface and the central portion of said first major surface; a second main electrode (19) formed on said second major surface of said first semiconductor layer; a second semiconductor layer (1; P); and,

an integral semi-insulating plasma CVD nitride film (14) covering at least the peripheral portion of said first major surface other than at least one specific central portion (the center portion that is directly under the opening 13) of said first major surface and not extending above at least one upper portion of the gate forming region in which the first gate(s) (such one upper portion of the gate forming region can be the upper portion(s) of the first gate(s) 8 that is/are directly under opening 13) is formed, said integral semi-insulating plasma CVD nitride film naturally having a conductivity which substantially does not lose function as an insulating film and substantially stabilizes breakdown voltage characteristics of the semiconductor device.

Regarding claims 3, 4, 8, 9, 14, 15, 19 and 20, the semiconductor device of AAPA further comprises a second gate (17) not covered with said first main electrode;

and a gate interconnection line (9) formed selectively on a surface of said second gate, wherein a trench is formed between said first main electrode and said gate interconnection line for electrical isolation between said first main electrode and said gate interconnect line, wherein said first gate and said second gate are integrally formed and electrically connected; and wherein said plasma CVD nitride film further extends from a surface of said gate interconnection line through said trench to a portion of a surface of said first main electrode.

Regarding claims 12-22, it is noted that each of the above identified regions can also be regarded as each being formed of multiple regions.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5, 6, 10, 11, 16, 17, 21 and 22, insofar as being in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA.

The disclosure of AAPA is discussed as applied to claims 1-4, 7-9, 12-15 and 18-20 above.

Although AAPA does not expressly disclose the specific conductivity for the semi-insulating nitride film, it is noted that the conductivity of such a nitride layer used for field relieving is an art-known resulted-oriented parameter of importance subject to

routine experimentation and optimization; and that these recited ranges of conductivity are well within (and/or, overlapping with) the art-known common range for the conductivity of such a nitride layer used for field relieving.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the device of AAPA with the conductivity of the semi-insulating nitride layer being formed within a range that is substantially within or overlapping with the one as that recited in the claims, so that a semiconductor device with optimized performance would be obtained, as it has been held that:

"[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Response to Arguments

Applicant's arguments filed on August 29, 2008 have been fully considered but they are not persuasive.

Applicant's main arguments include: applicant's admitted prior art ("AAPA") does not disclose the claimed invention, especially that of the recited nitride film and its positional relationship with the first gate(s). In response it is noted that, insofar as being in compliance with 35 U.S.C. 112, the integral semi-insulating plasma CVD nitride film (14) in AAPA does cover at least the peripheral portion of said first major surface, but not cover at least one specific central portion (i.e., the specific center portion that is directly under the opening 13) of the first major surface and does not extend above **at**

least one specific upper portion of the gate forming region, wherein such specific one upper portion of the gate forming region can be any upper portion (such as a fraction) of the first gate or gates (8) that is/are directly under the opening 13, regardless whether or not it (the integral semi-insulating plasma CVD nitride film 14) may also extend above any other upper portion(s) of the first gate or gates, given that the claims are in an open-ended manner, which does not exclude any other extension(s) for the recited integral semi-insulating plasma CVD nitride film in the claims.

Applicant's arguments appear to intend to imply that AAPA fails to show the feature of the instant invention that the integral semi-insulating plasma CVD nitride film does not extend above **any upper portion** of **any first gate or gates** in the claimed device. However, it is noted that such features upon which applicant relies are not recited in the rejected claim(s), which is especially true as the term of "an upper portion of the gate forming region" does not necessary have to be interpreted as meaning: the entire upper surface of the entire first gate forming region. Applicant is reminded that: Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Response to applicant's other arguments have been fully incorporated into the claims rejections and/or objections set forth above in this office action.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Friday, 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Shouxiang Hu/
Primary Examiner, Art Unit 2811